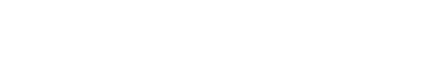
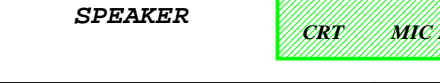
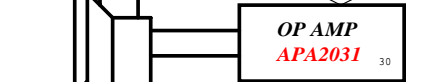
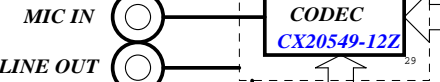
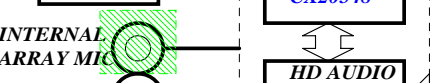
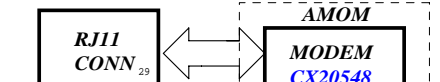
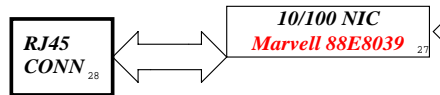
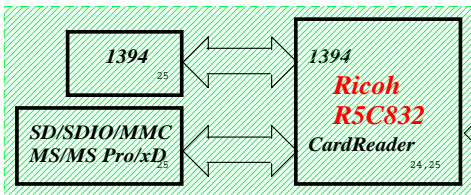
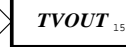
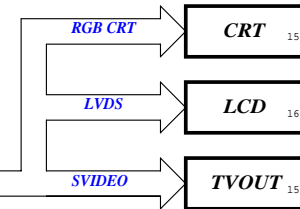
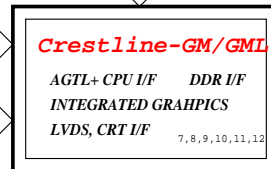
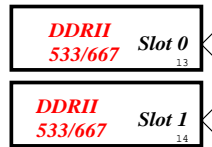
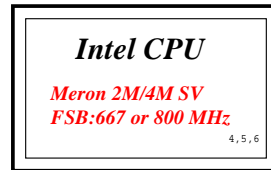


# Pamirs UMA Block Diagram

Project code : 91.4S401.001

PCB P/N : 06228

Revision : SB



Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN. NOTE: This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h: bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05, VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL. Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. (Offset: 3410h: bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up. If sampled low, the Flash Descriptor Security will be overridden. If high, the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP#3	AZ DOUT ICH	Description	
0	0	RSVP	
0	1	Enter XOR Chain	
1	0	Normal Operation (default)	
1	1	Set PCIE port cofin bit	

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSus1_05, VccSus1_5, VccCL1_5			
SM_INTVRMEN	High=Enable	Low=Disable	
Integrated VccLAN1_05 VccCL1_05			
LAN100_SLP	High=Enable	Low=Disable	

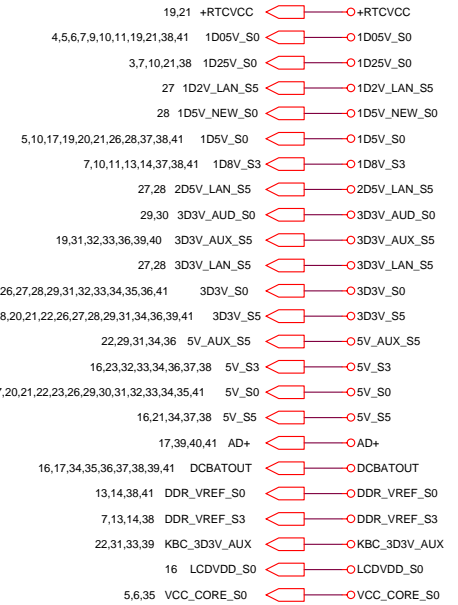
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

## INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

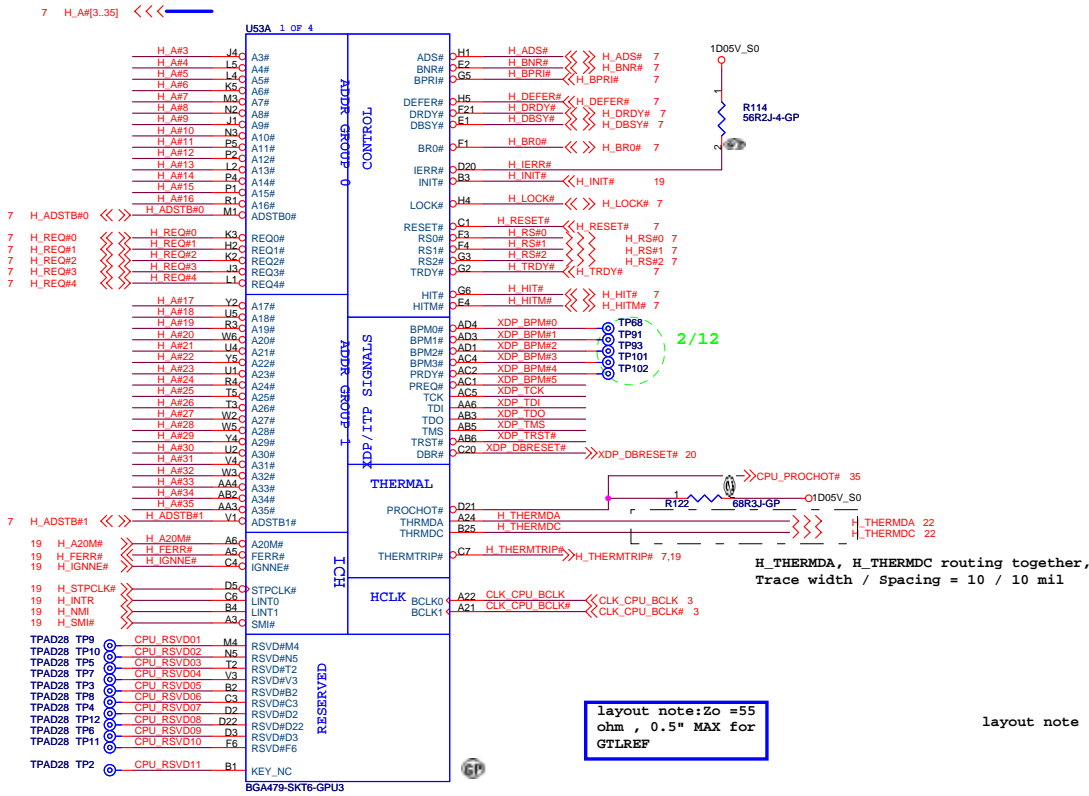


## INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 8 Low Power PCI Express	Normal	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode (Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled
CFG 19 DMI Lane Reserved	Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13	Reserved	
LH(0)	Reserved	
LH(1)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HL(11)	Normal Operation	

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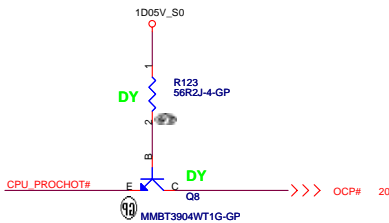
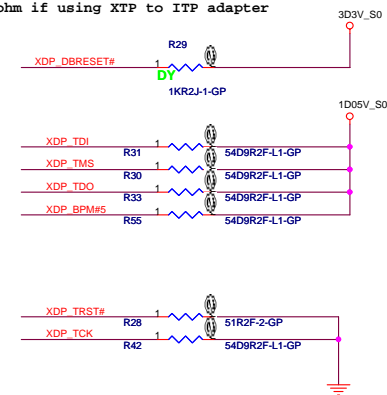




original value: BGA479-SKT6-GPU1

layout note: Zo = 55 ohm, 0.5\"/>

layout note : Change R237 to 649 ohm if using XTP to ITP adapter

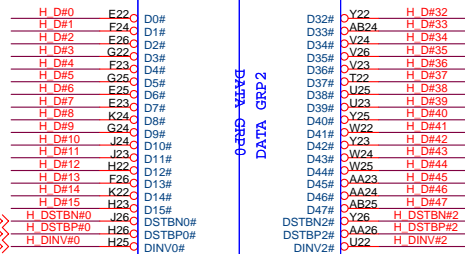


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Title			
Meron(1/3)-AGTL+XDP			
Size	Document Number	Rev	
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7 H\_DW[0..63] <<>>

U53B 2 OF 4



7 H\_DSTBN#0  
7 H\_DSTBN#1  
7 H\_DIN#0

7 H\_DSTBN#1  
7 H\_DSTBN#2  
7 H\_DIN#1

V CPU\_GTLREF

TPAD28 TP13

TPAD28 TP16

TPAD28 TP14

TPAD28 TP15

TPAD28 TP1

TPAD28 TP15

TPAD28 TP15

TPAD28 TP15

TPAD28 TP15

TPAD28 TP15

TPAD28 TP15

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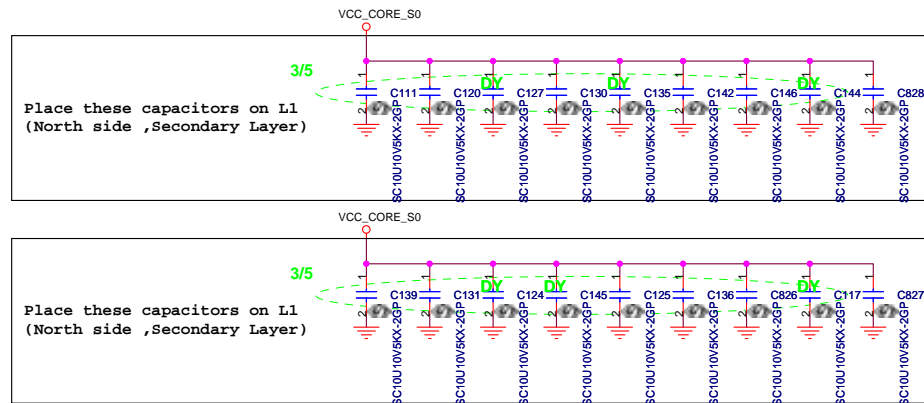
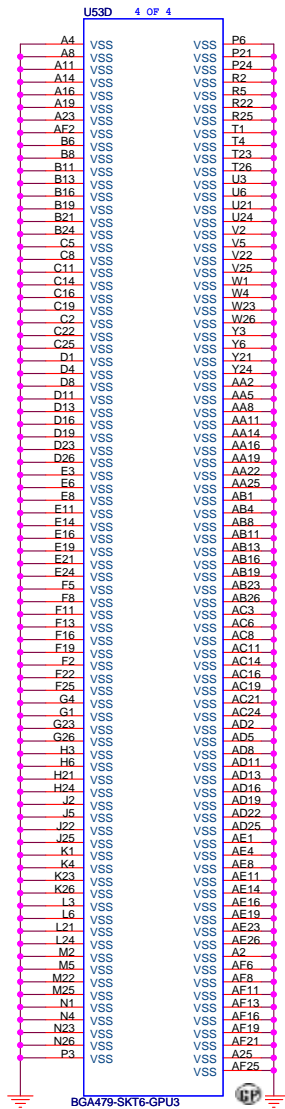
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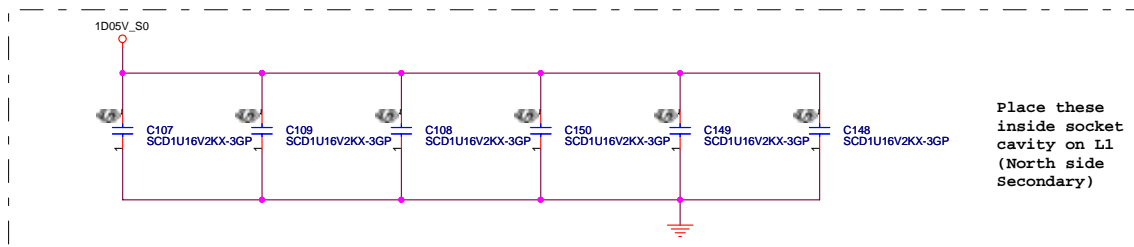
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TPAD28 TP15



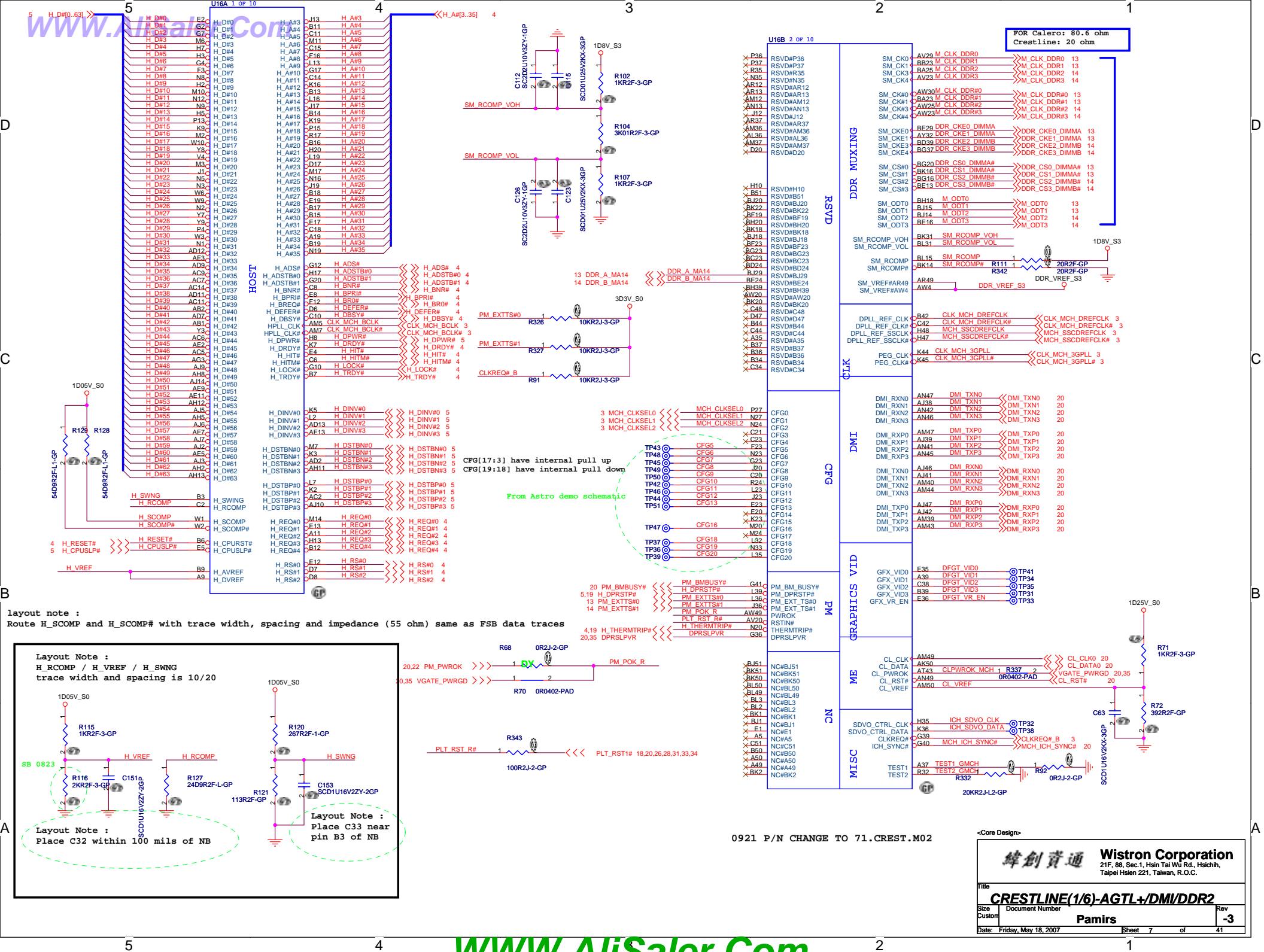
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Decoupling

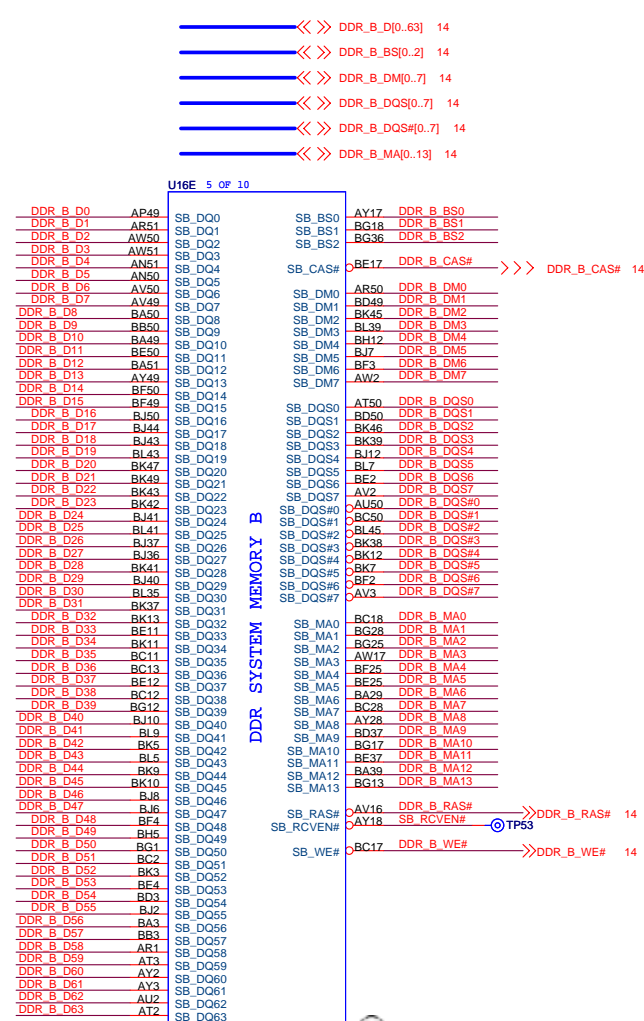


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<p>Title</p> <p><b>Meron(3/3)-GND&amp;Bypass</b></p>	
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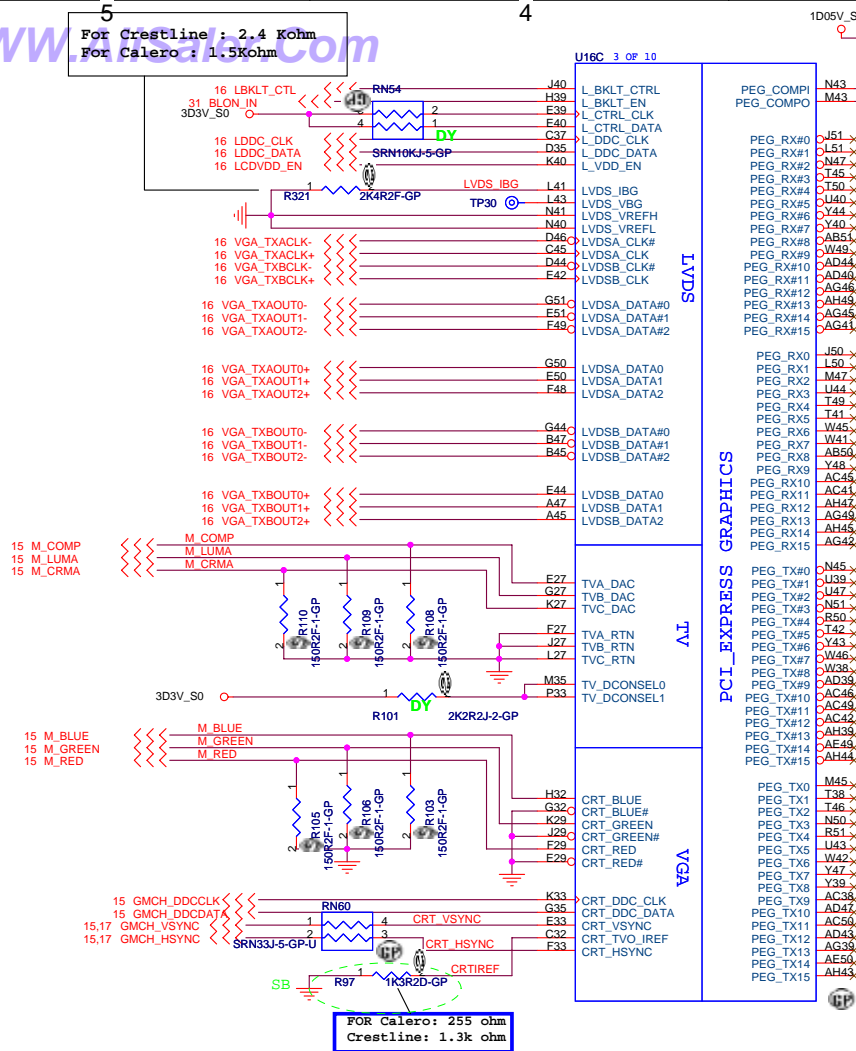






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Title	
<b>CRESTLINE(2/6)-DDR2 A/B CH</b>	
Size A3	Document Number <b>Pamirs</b>
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## Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

&lt;Core Design&gt;

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Title
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**CRESTLINE(3/6)-VGA/LVDS/TV**

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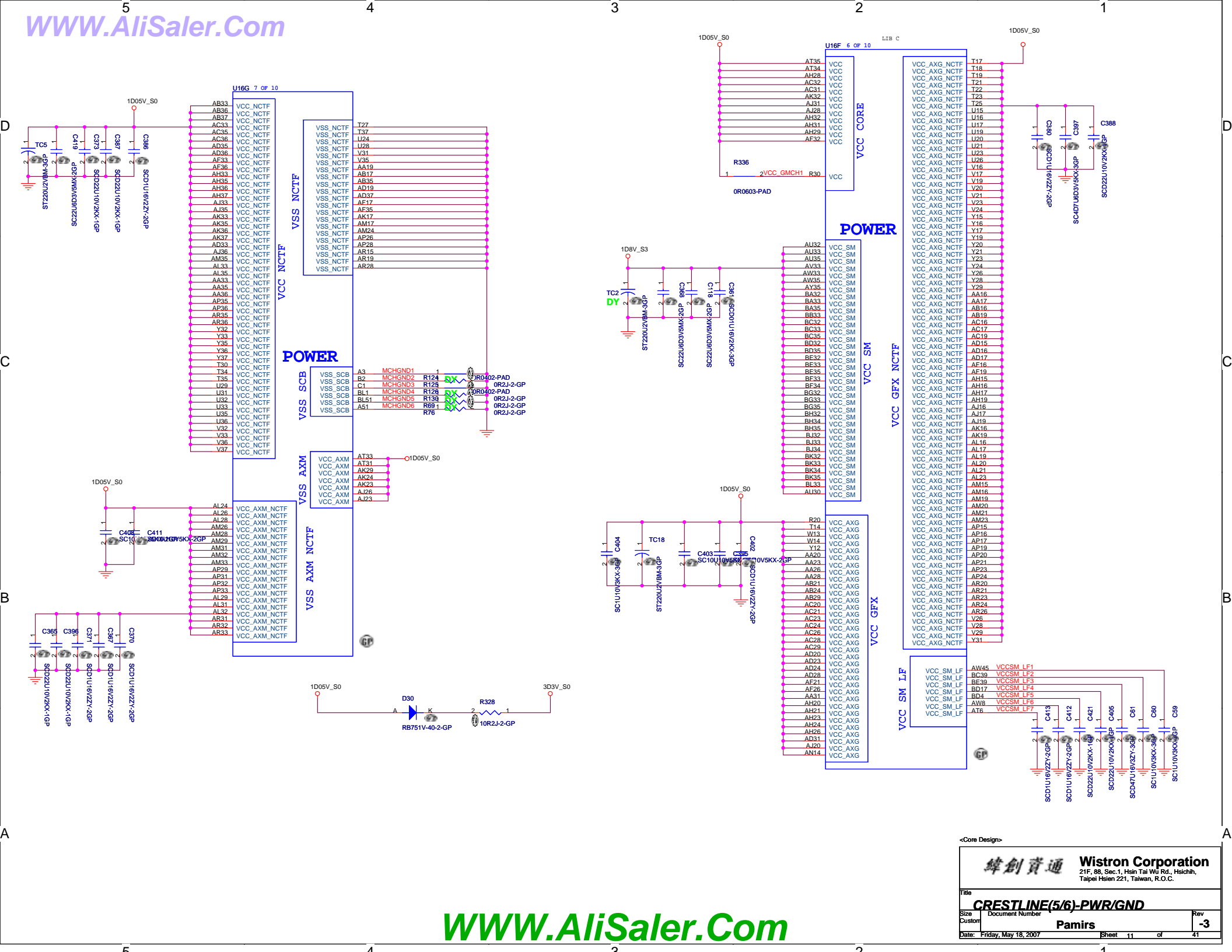
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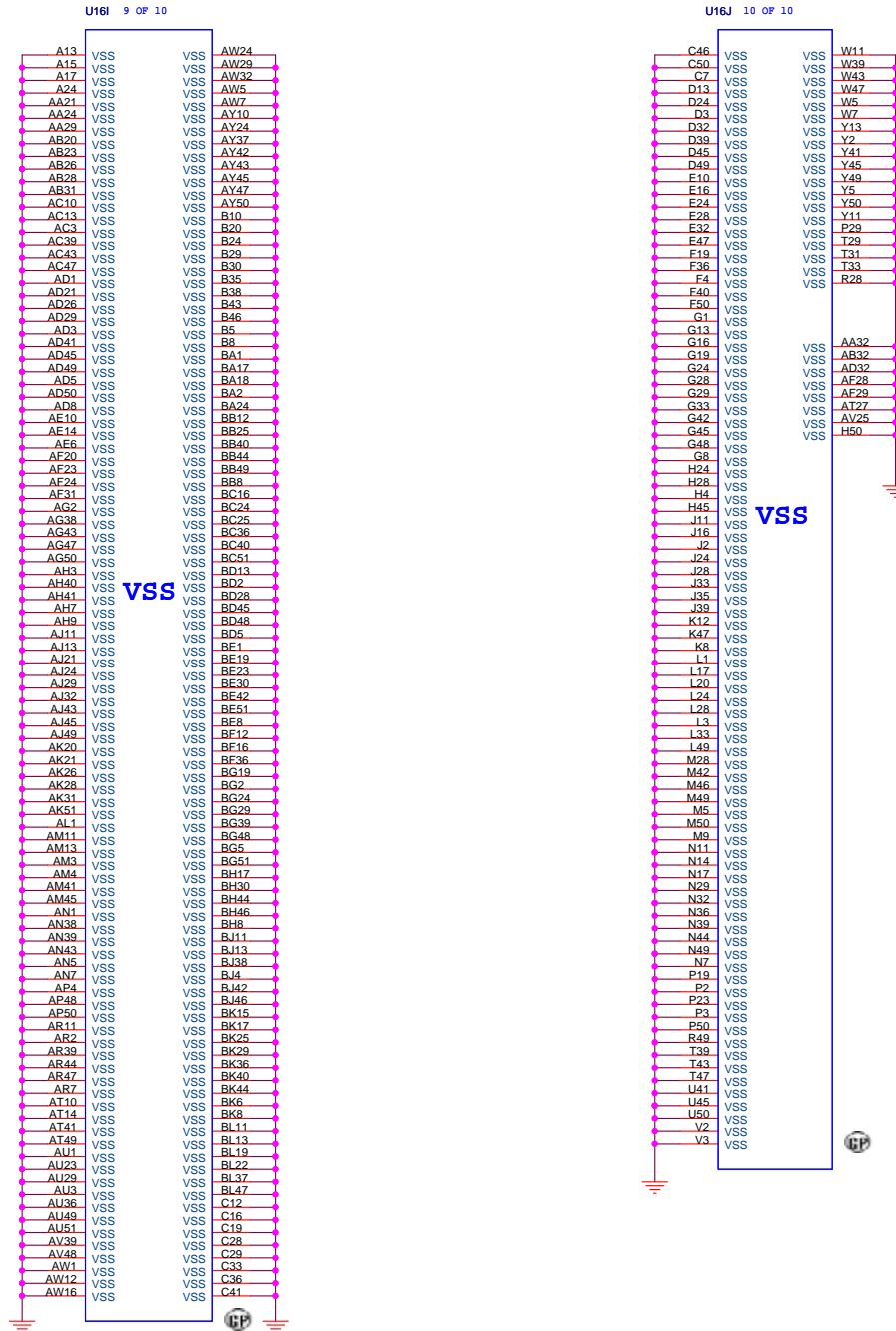
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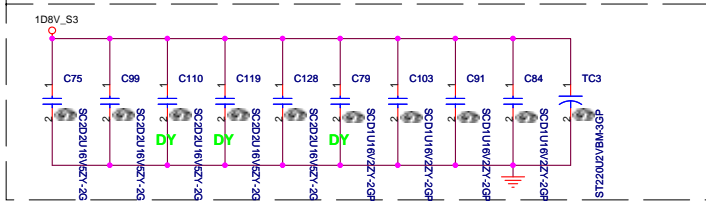


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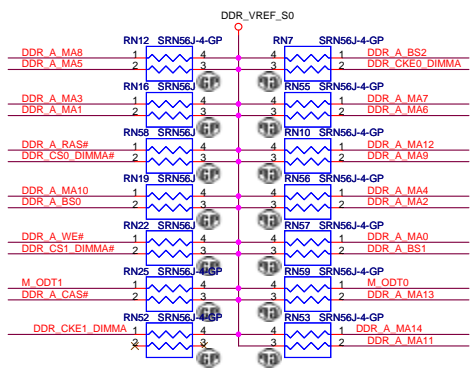
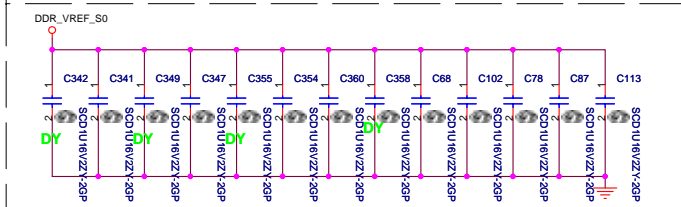
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Size A3	Document Number <b>Pamirs</b>
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8 DDR\_A\_DQS[0..7] <<>>  
 8 DDR\_A\_D[0..63] <<>>  
 8 DDR\_A\_DM[0..7] <<>>  
 8 DDR\_A\_DQS[0..7] <<>>  
 8 DDR\_A\_MA[0..13] <<>>  
 8 DDR\_A\_BS[0..2] <<>>

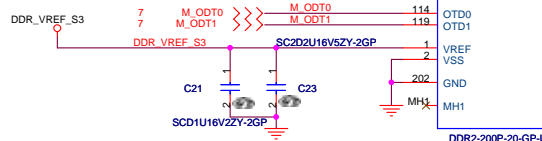
Layout Note:  
Place near DM1



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:  
Place these resistors  
closely DM1,all  
trace length Max=1.5"



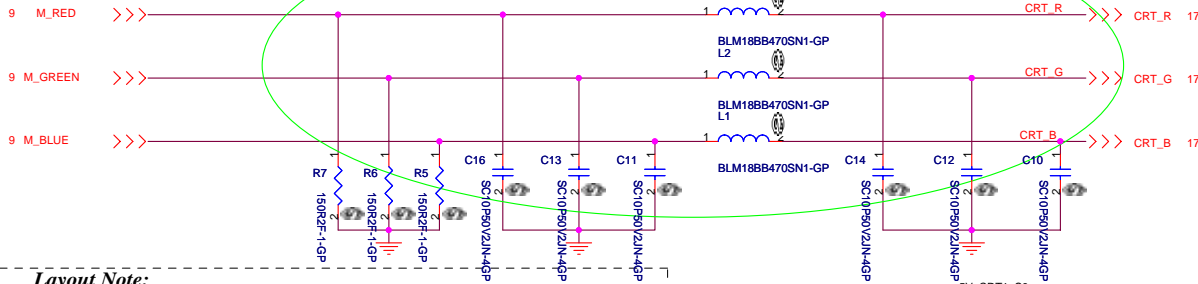
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 DDR\_A\_MA4 98 A4  
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 DDR\_A\_MA6 96 A6  
 DDR\_A\_MA7 95 A7  
 DDR\_A\_MA8 94 A8  
 DDR\_A\_MA9 93 A9  
 DDR\_A\_MA10 92 A10/AP  
 DDR\_A\_MA11 91 A11  
 DDR\_A\_MA12 90 A12  
 DDR\_A\_MA13 89 A13  
 DDR\_A\_MA14 88 A14  
 DDR\_A\_MA15 87 A15  
 DDR\_A\_MA16 86 A16/BA2  
 DDR\_A\_MA17 85 A17  
 DDR\_A\_MA18 84 A18  
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 DDR\_A\_MA20 82 A20  
 DDR\_A\_MA21 81 A21  
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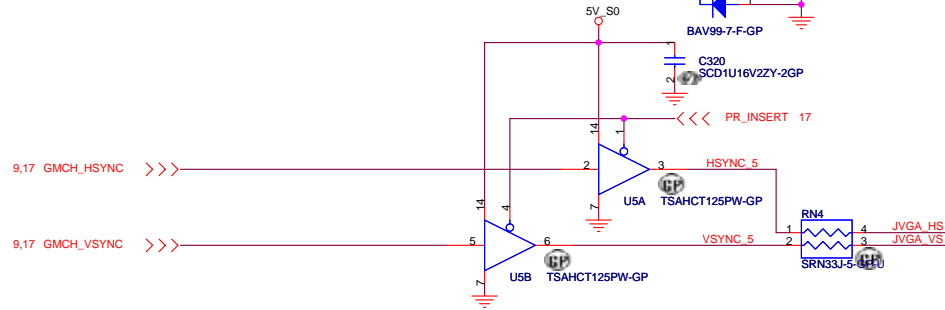
# CRT I/F & CONNECTOR

Layout Note:  
Place these resistors  
close to the CRT-out  
connector



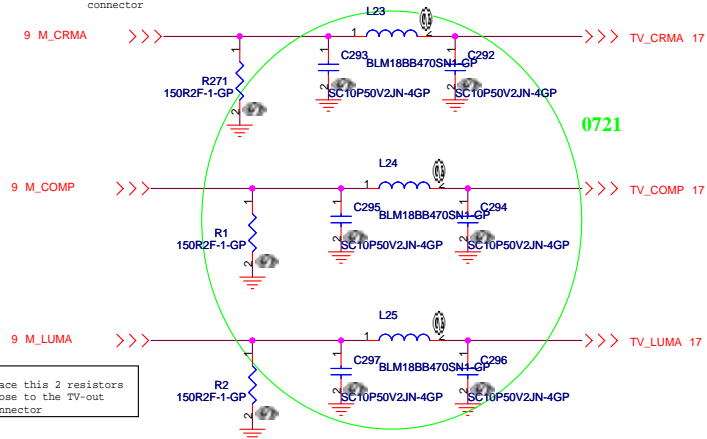
**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

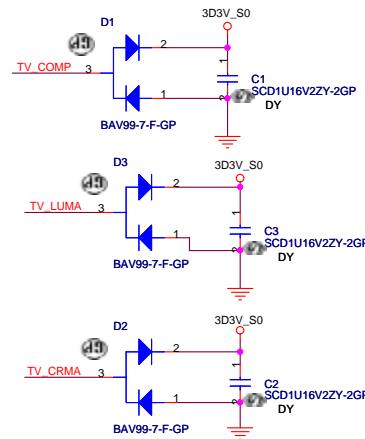
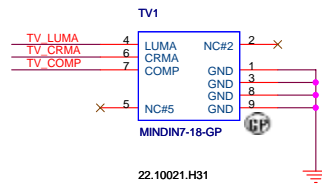


## TV OUT CONN

connector



Place this 2 resistors  
close to the TV-out  
connector



<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

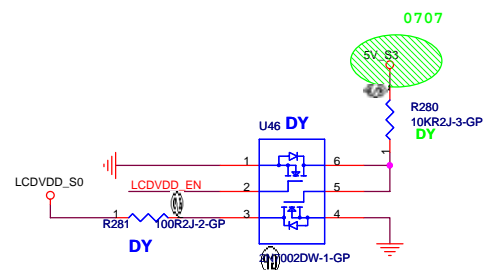
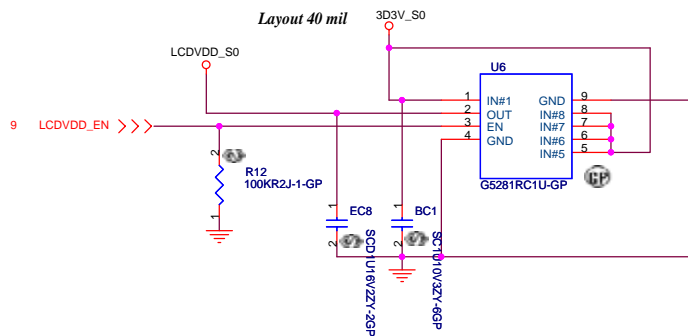
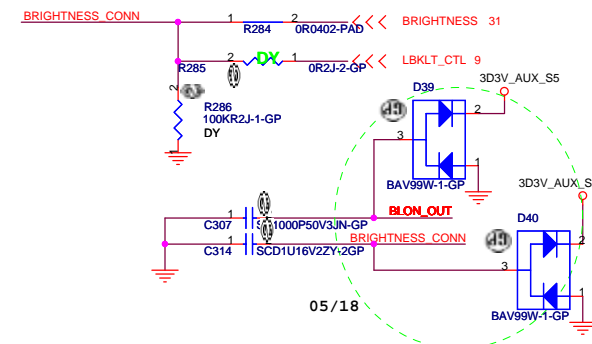
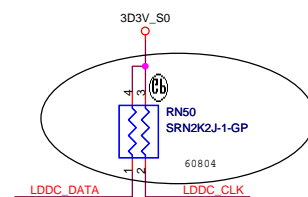
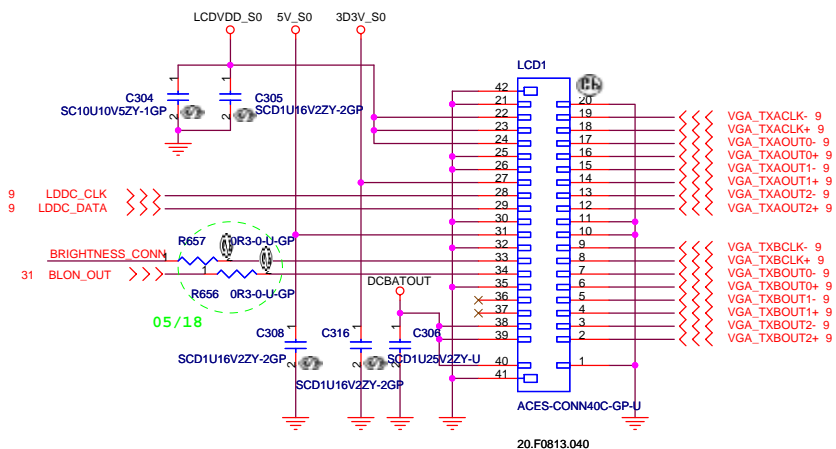
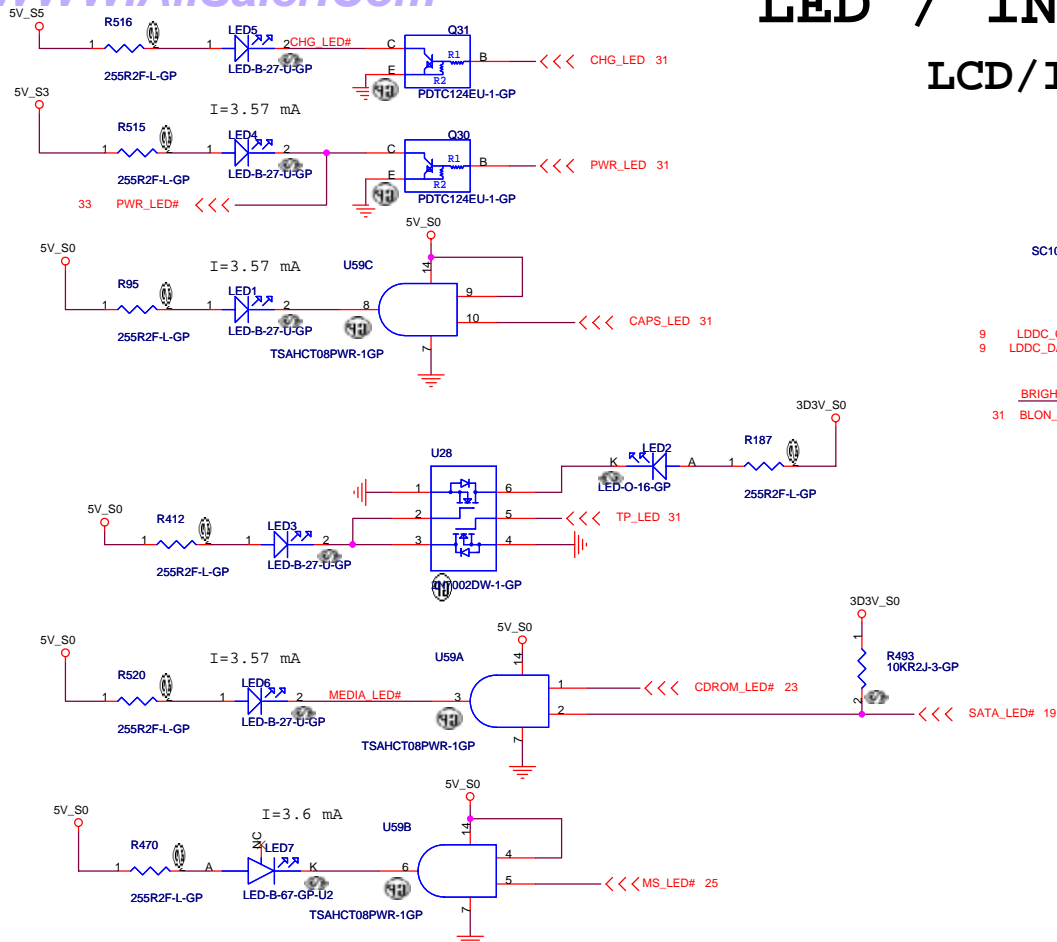
Title: **CRT/TV Connector**

Size A3 Document Number: **Pamirs** Rev: **-3**

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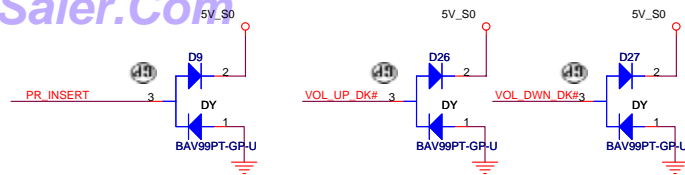
# LED / INVERTER INTERFACE

## LCD/INV CONN

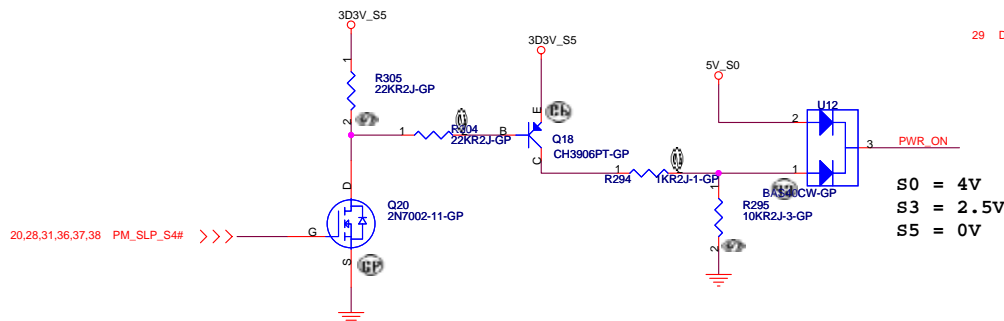
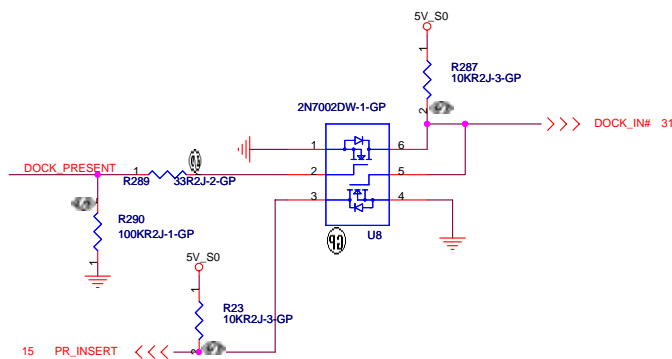
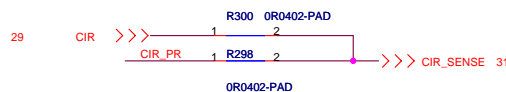
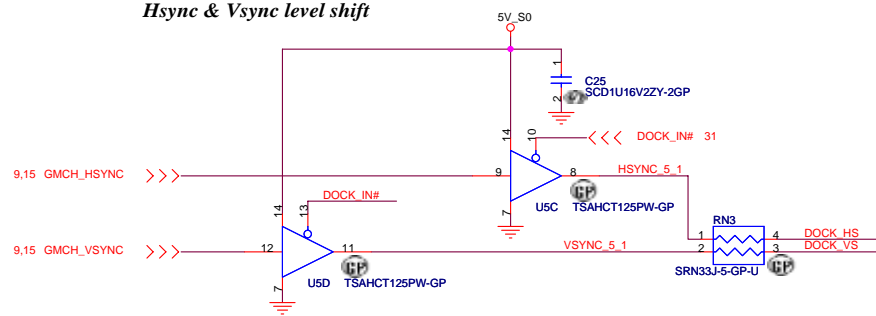


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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LCD/Inverter Connector			
Size Custom	Document Number	Pamirs	Rev -3
Date:	Monday, May 21, 2007	Sheet 16 of	41

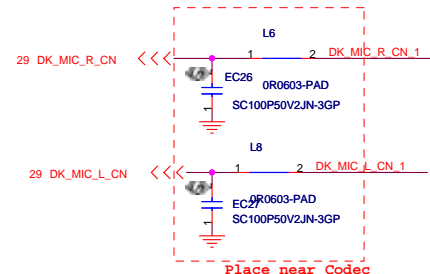
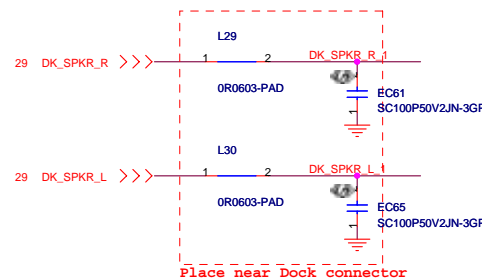
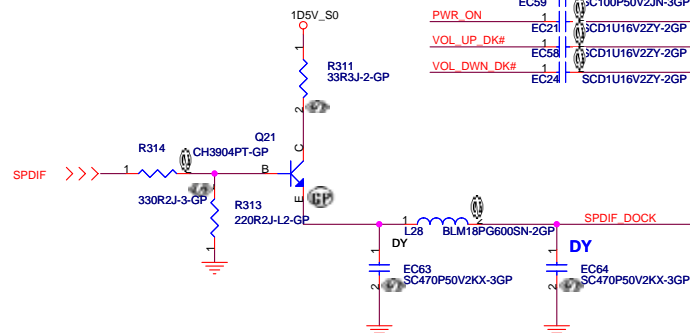
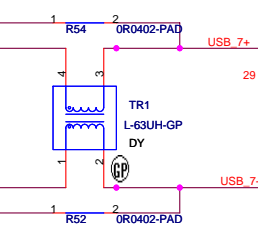
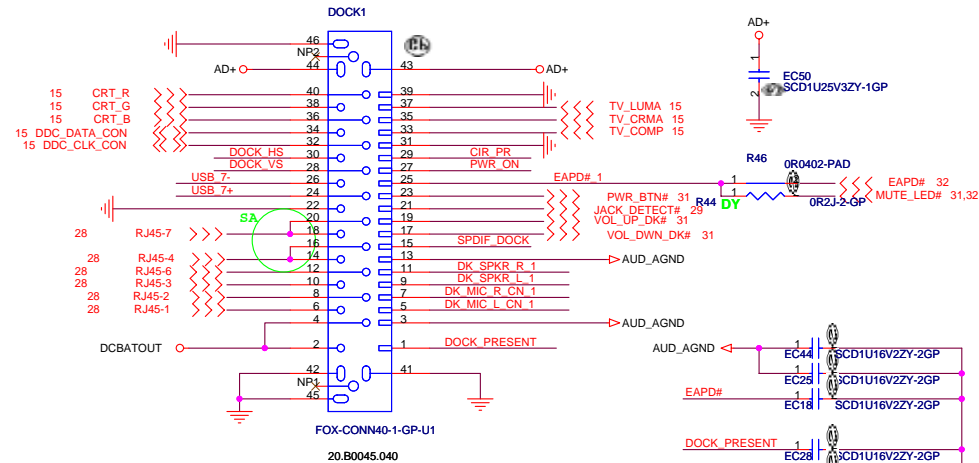
# Docking Connector



## Hsync & Vsync level shift

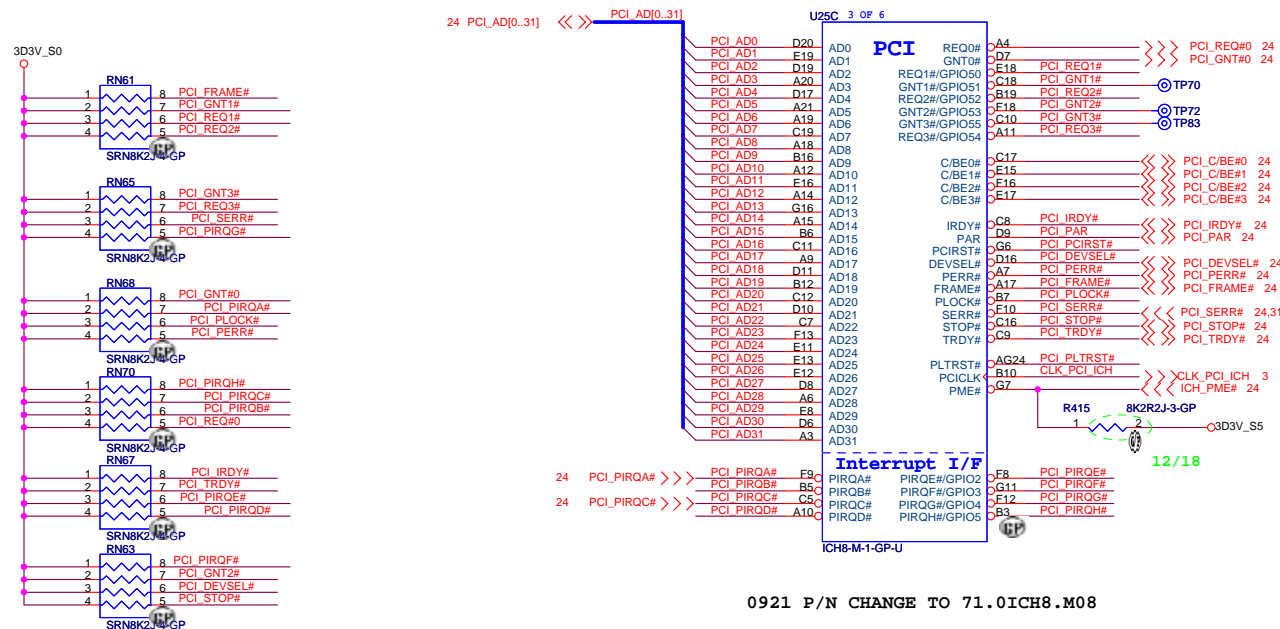


S0 = 4V  
S3 = 2.5V  
S5 = 0V



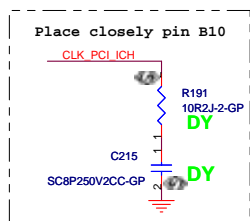
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<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	<b>Board to board conn/ Docking</b>
Size A3	Document Number
Date: Friday, May 18, 2007	Rev -3
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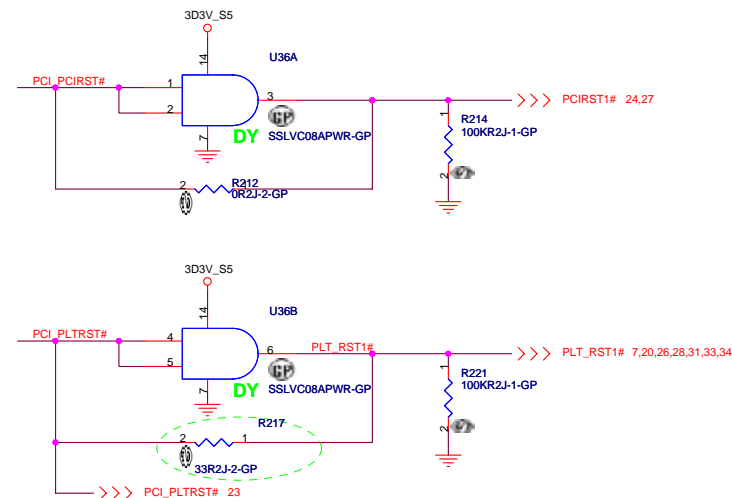


0921 P/N CHANGE TO 71.0ICH8.M08

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



<Variant Name>

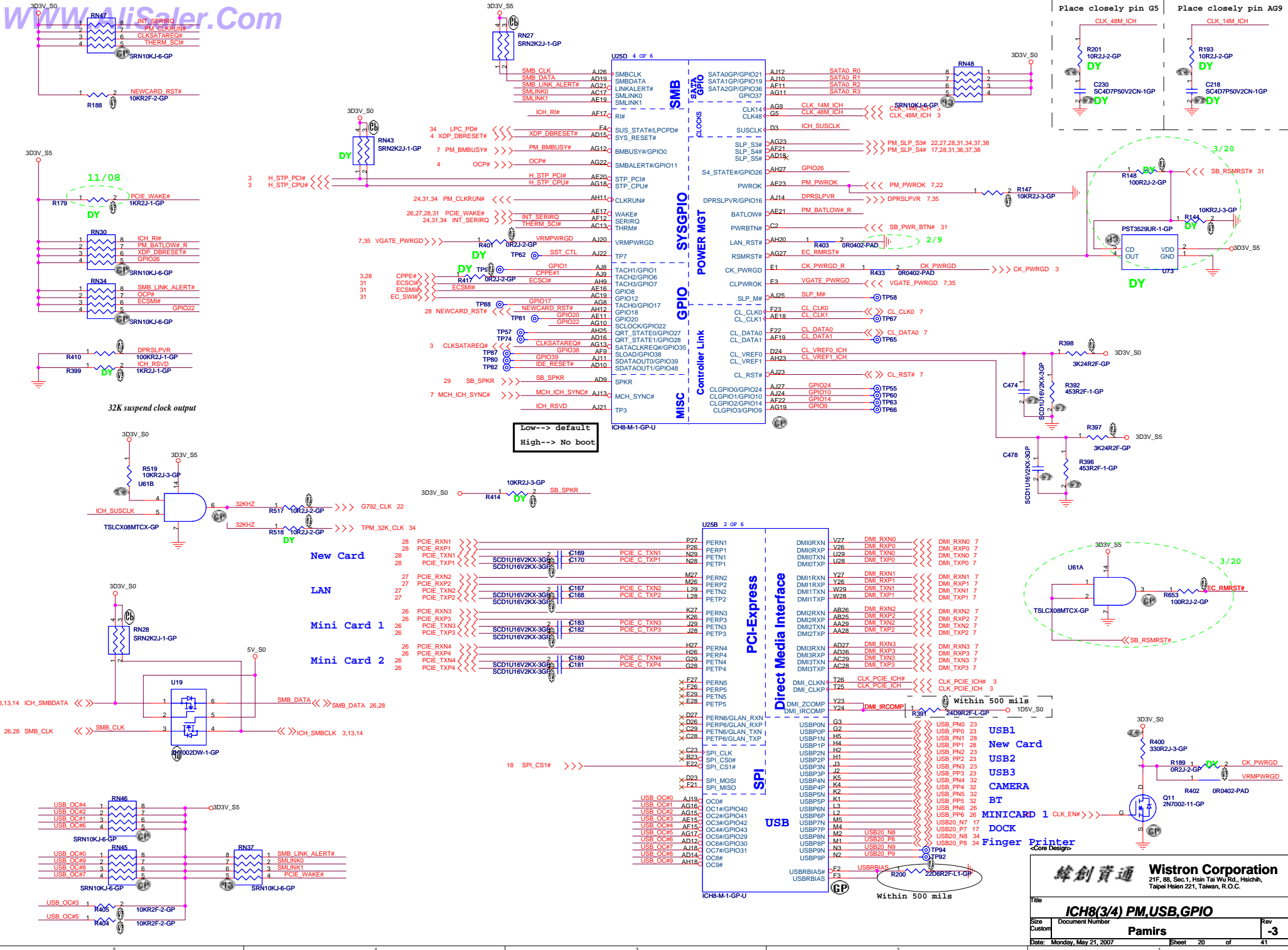
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH8(1/4)-PCI/INT**

Size: A3 Document Number: **Pamirs** Rev: **-3**

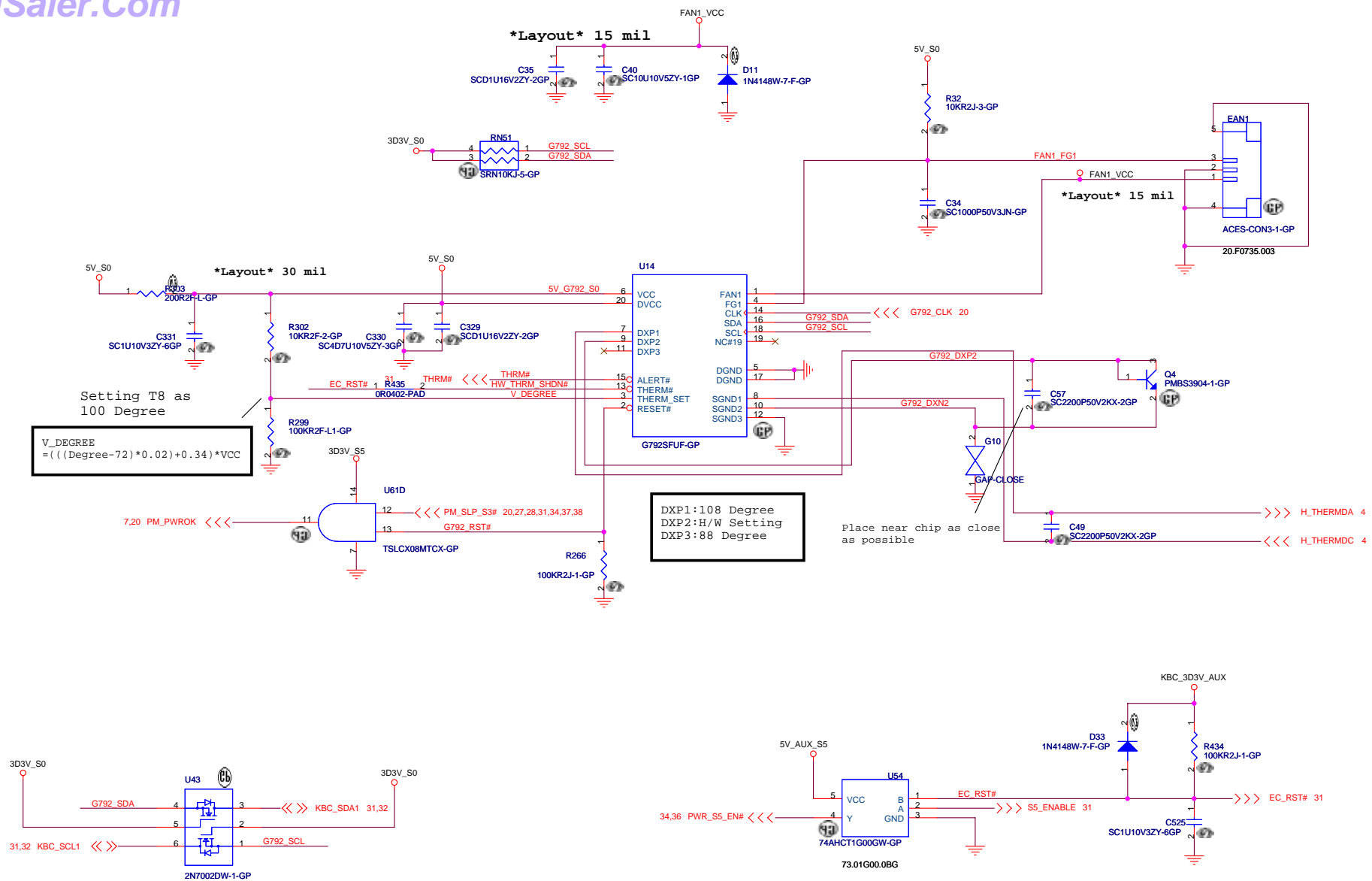
Date: Friday, May 18, 2007 Sheet: 18 of 41







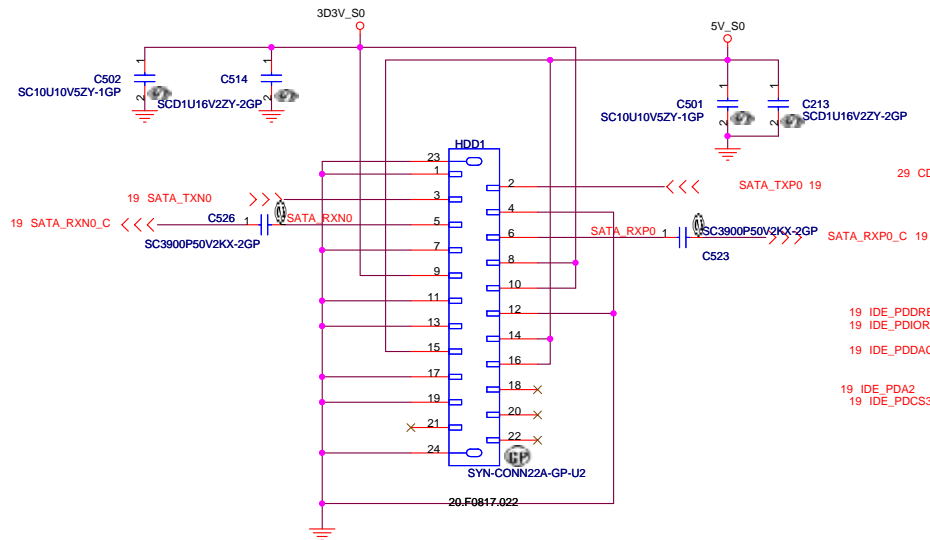




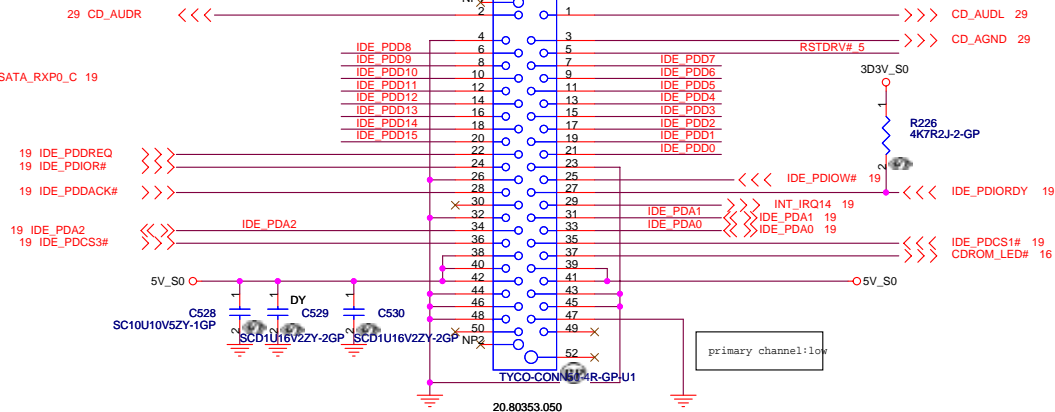
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<p><b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title <b>Thermal/Fan Controller G792</b></p>	
Size Custom	Document Number <b>Pamirs</b>
Date: Monday, May 21, 2007	Rev <b>-3</b>
<p>Sheet 22 of 41</p>	

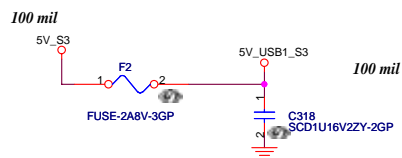
## SATA HD Connector



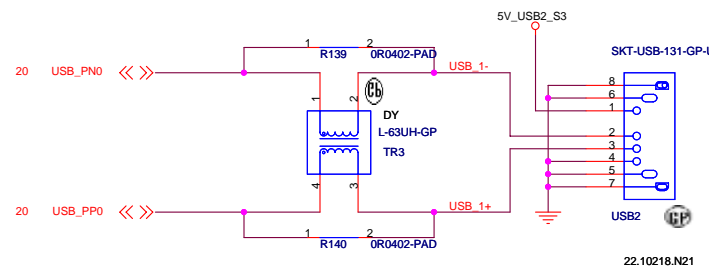
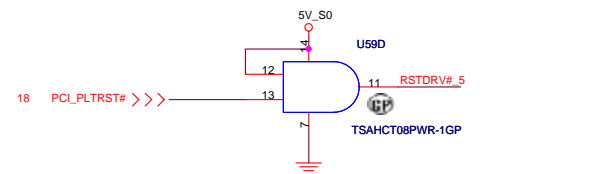
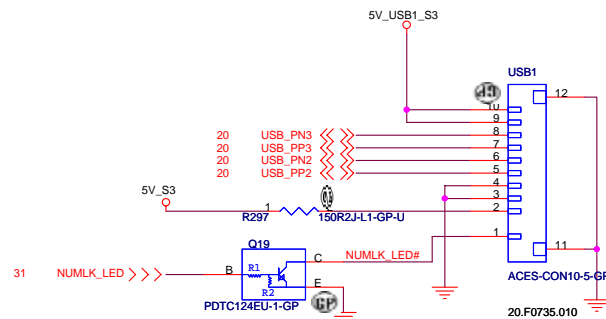
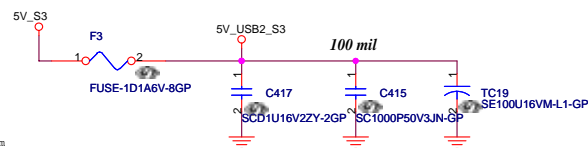
## CD-ROM CONNECTOR



## USB PORT

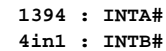


High limit under 2.5 mm



<Core Design>

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<b>HD/CDROM/USB</b>	
Title Size A3 Date: Friday, May 18, 2007	Document Number <b>Pamirs</b> Sheet 23 of 41
Rev <b>-3</b>	



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Taipei Hsien 221, Taiwan, R.O.C.

**R5C832/PCI**

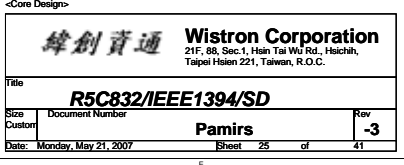
Rev	
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## Pamirs

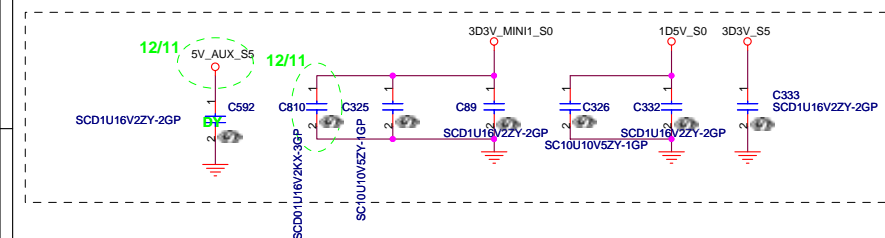
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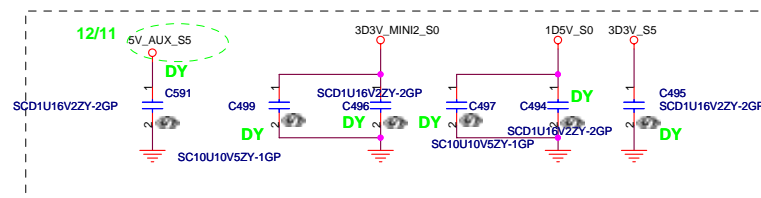
Sheet 24 of 41



### ***Mini Card Connector 1(WWAN)***

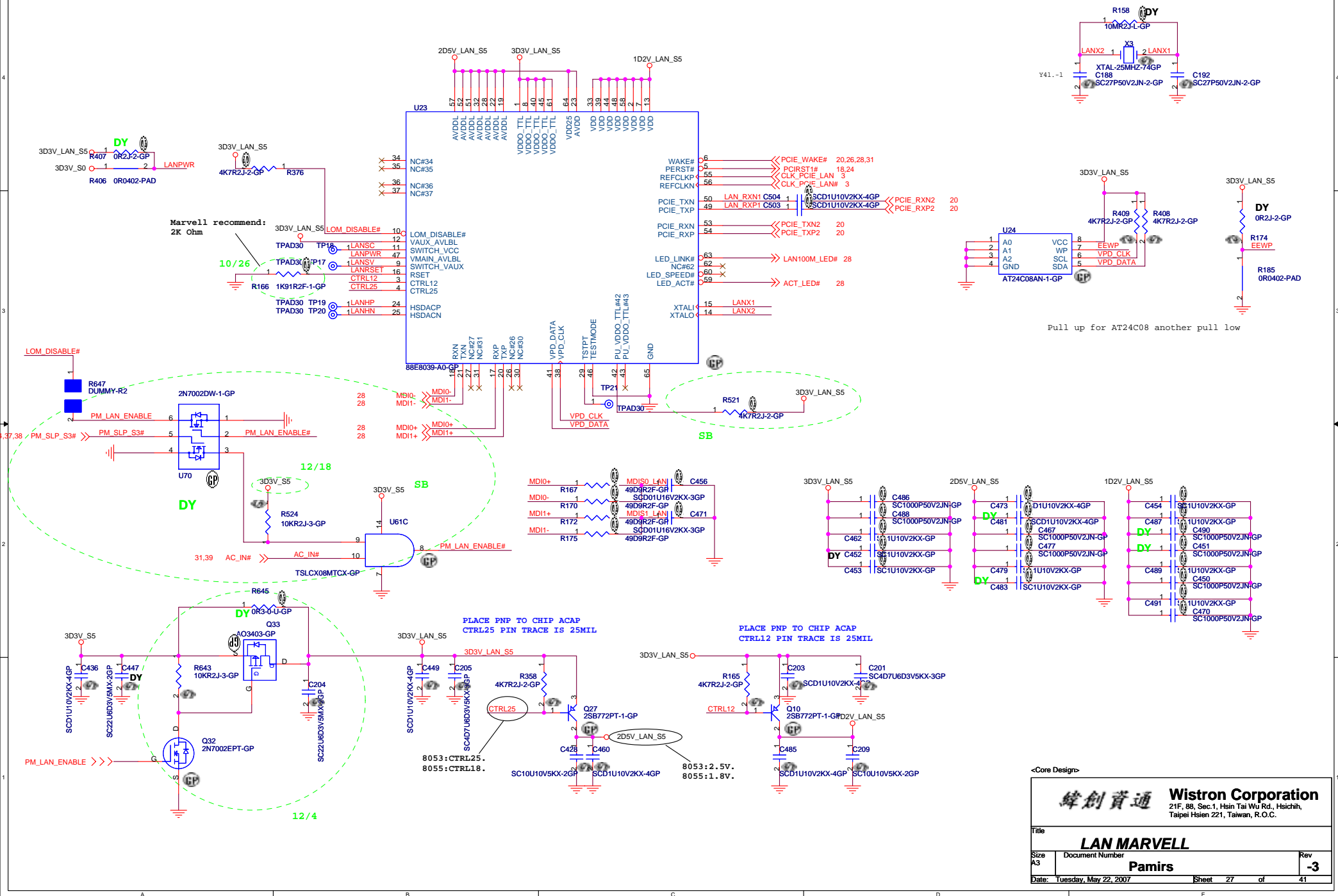


### *Mini Card Connector 2(802.11a/b/g)*

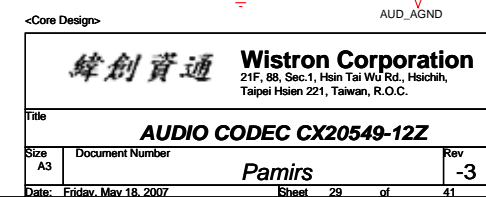


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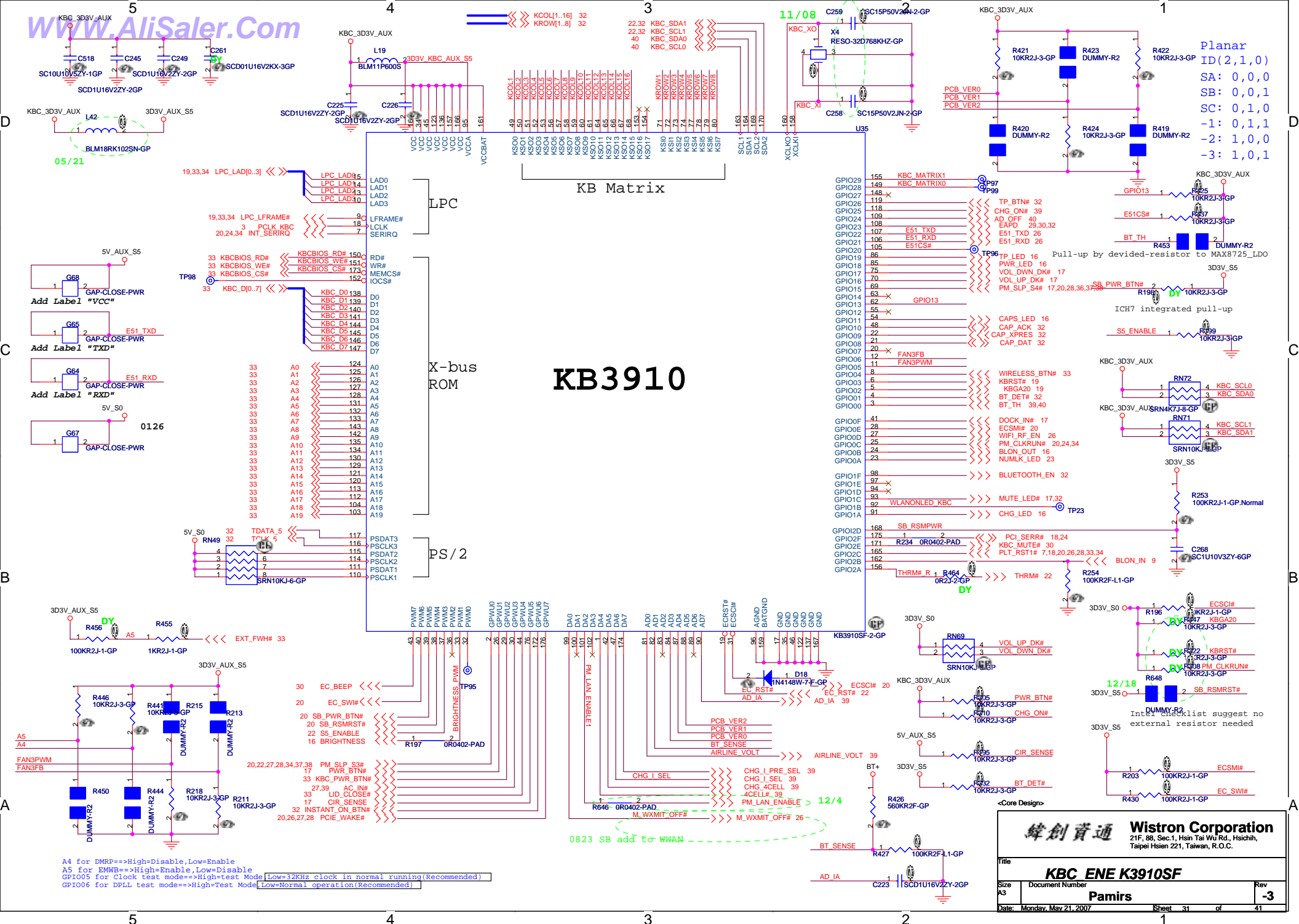












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**KBC ENE K3910SF**

**Pamirs**

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# CAMERA

# Blue thumb

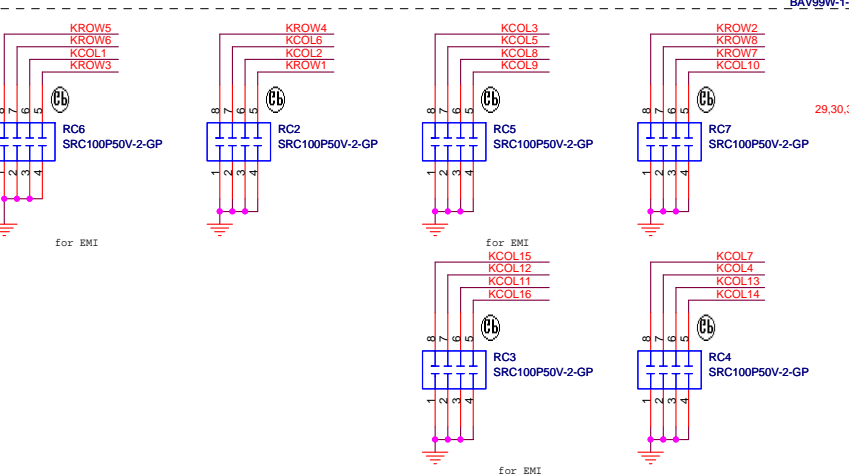
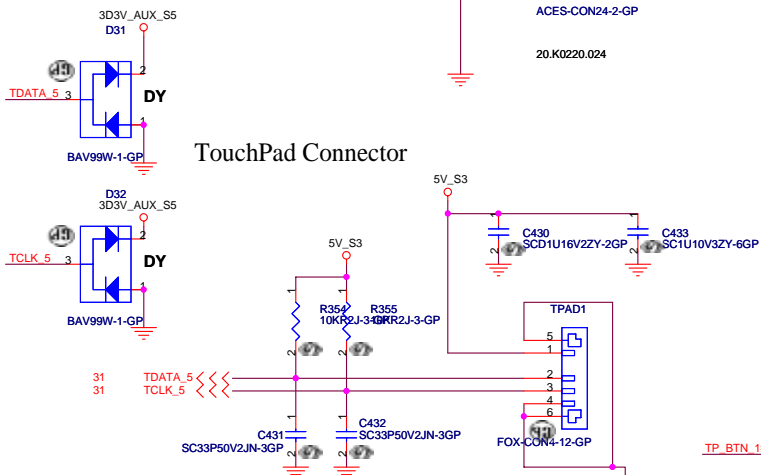
## Internal KeyBoard Connector

31 KROW[1..8] <<< <<<  
31 KCOL[1..16] <<< <<<

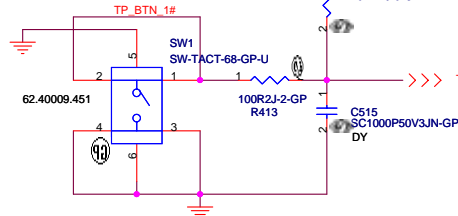
Keyboard matrix ( from vendor )

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

## TouchPad Connector



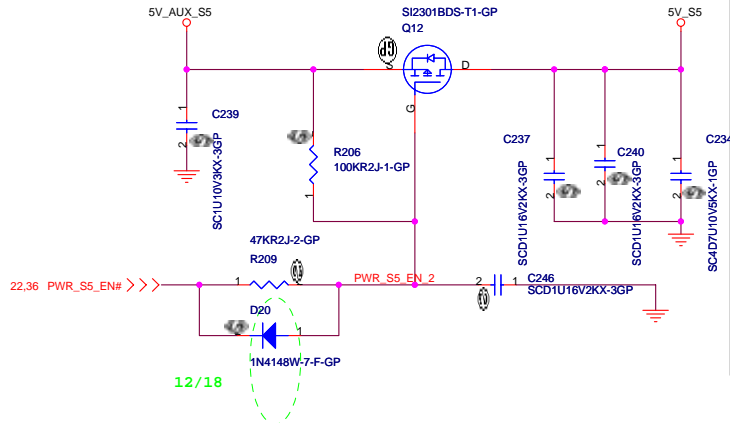
## TOUCH-PAD SWITCH



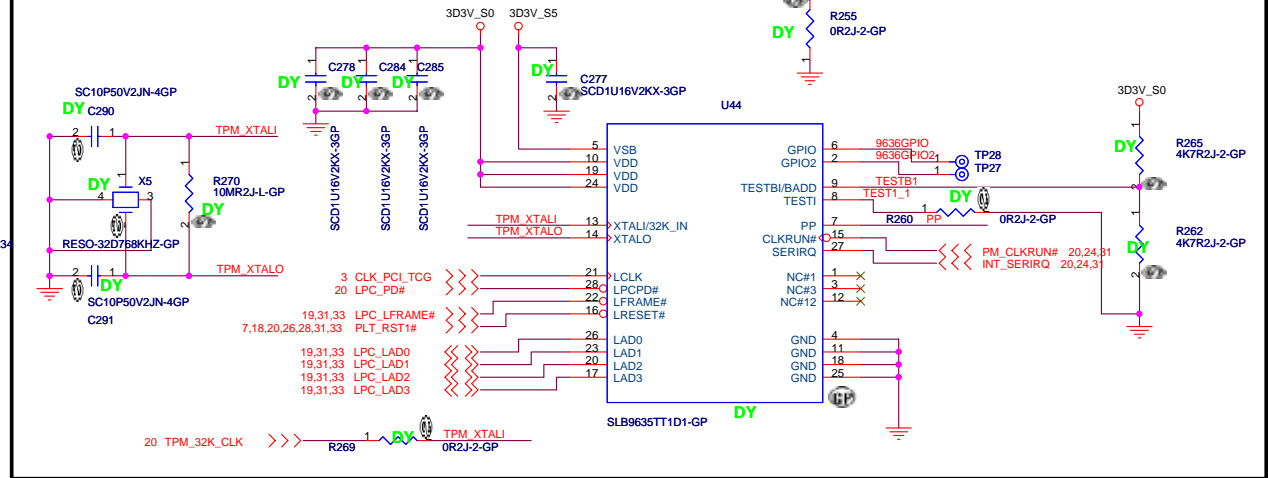




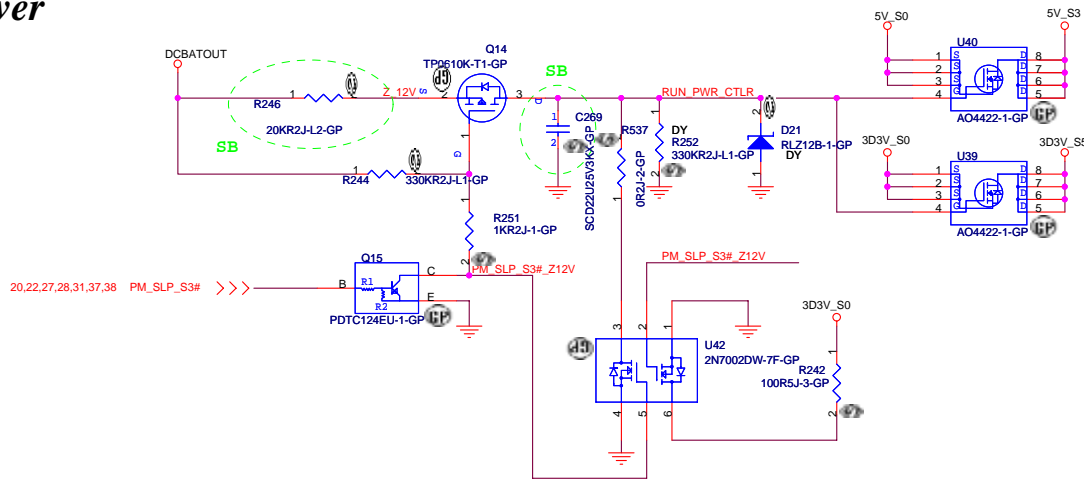
## 5V\_AUX\_S5 TO 5V\_S5



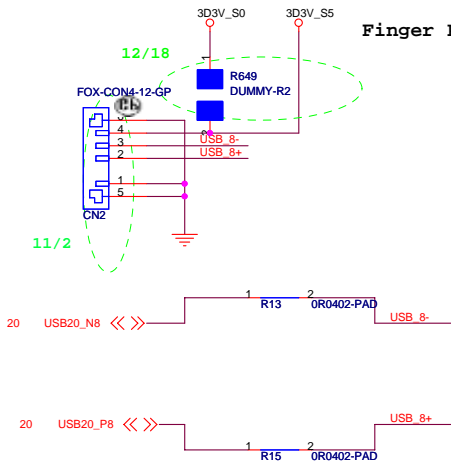
## TPM 1.2



## Run Power

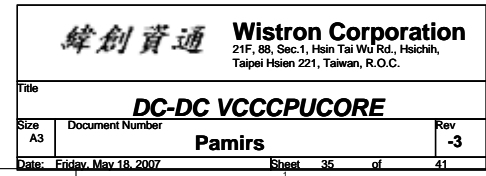


## Finger Printer



<Core Design>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>PWRPLANE&amp;RESETLOGIC</b>		
Size A3	Document Number	Rev
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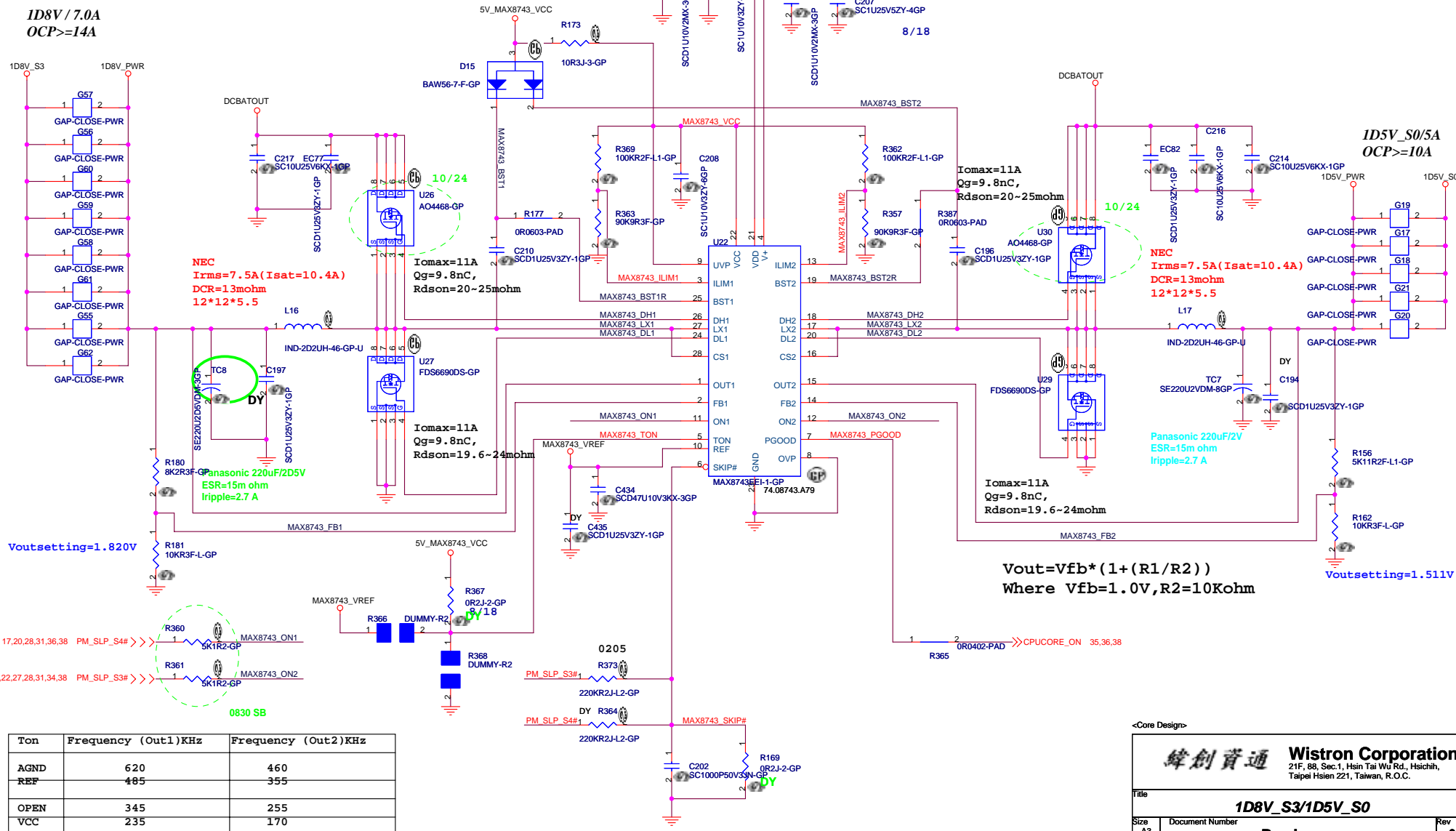




$$\begin{aligned} I_{ocp} &= 7.0 \times 2 = 14A \\ R_{ds,on} &= 17m \text{ ohm} \\ V_{cs2} &= I_{ocp} \times R_{ds,on} = 28mV \\ V_{ILIM2} &= V_{cs2} / 0.1 = 2.38V \end{aligned}$$



**1D8V / 7.0A**  
**OCP>=14A**



Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

&lt;Core Design&gt;

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**1D8V\_S3/1D5V\_S0**

Size

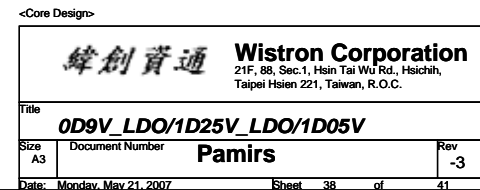
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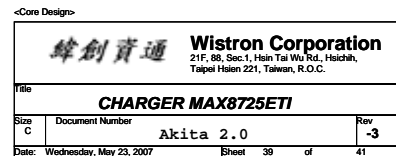
## Pamirs

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**New**









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Taipei Hsien 221, Taiwan, R.O.C.

Title
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**AD/BATT CONN**

Size

Document Number
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Akita 2.0

Rev

Date: Friday, May 18, 2007

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